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Research of integrated digital decimation filters

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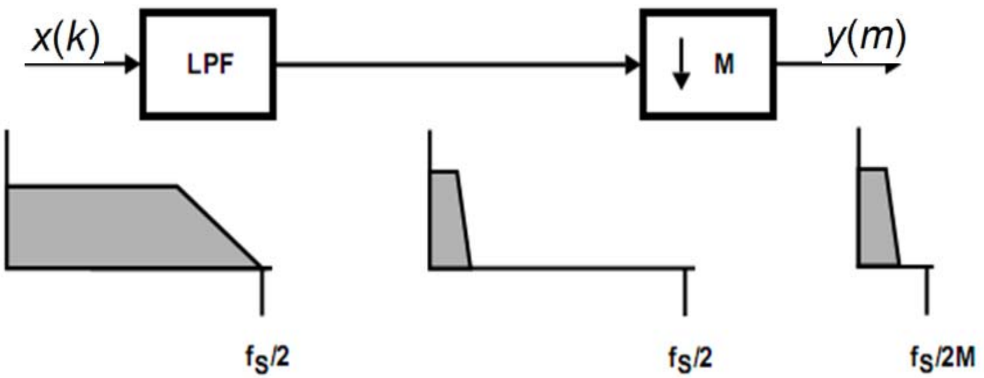
INTRODUCTION

In digital signal processing, decimation is technique for reducing the number of samples in a discrete-time signal.

Decimation is a two-step process:

- Low-pass anti-aliasing filter
- Downsampling



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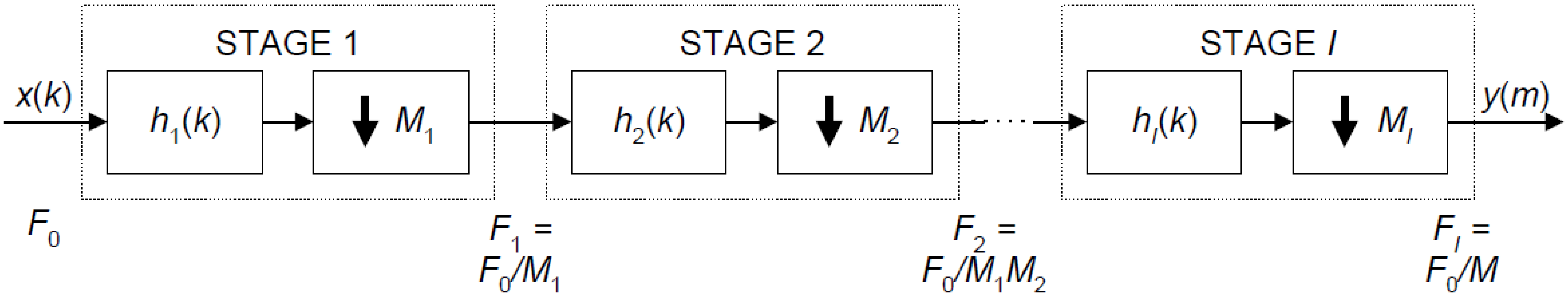
MULTISTAGE DECIMATORS

- A decimation filter can be realized by cascading several stages
- The decimation ratio must be factored into the product of integer numbers

$$M = \prod_{i=1}^{I} M_i$$



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TYPES OF DECIMATION FILTERS

CIC-filters

- Multiply-free filters
- Not need a complex synchronization and large external control
- Narrow pass-band in relation to the sample rate
- The width of registers increases with increase in factor frequency change.

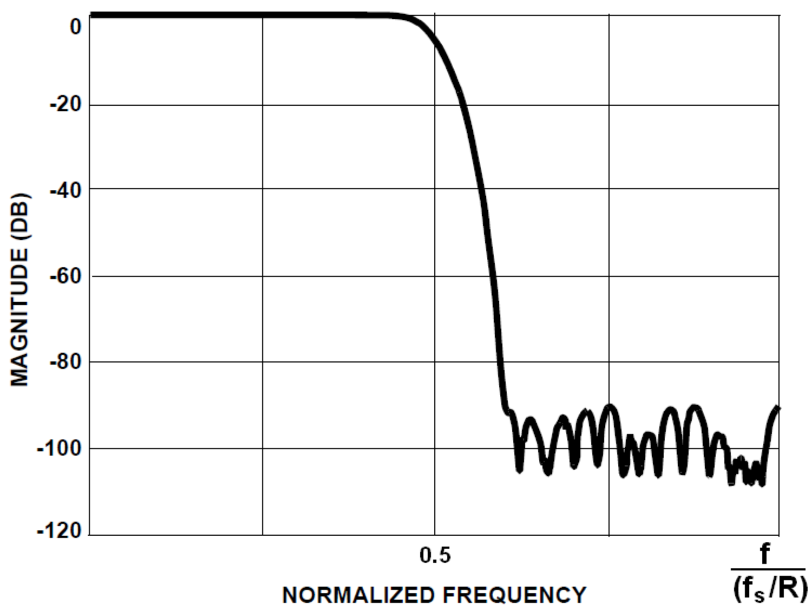
Halfband-filters

- Flat frequency response
- Difficult enough management
- Contain in its structure multipliers
- Bad suppression in the stop-band

The general filter used in PDC designs is a halfband product. The halfband is also typically implemented as a fixed coefficient filter, however it also represents a less efficient implementation than the CIC. Its frequency response is characterized by a very flat pass-band.

FILTERS FREQUECY RESPONSES

Halfband

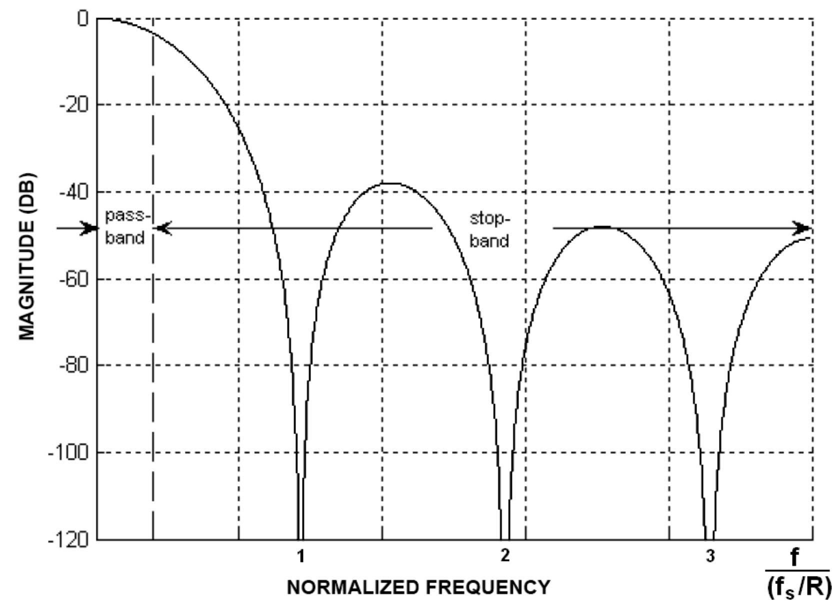


R = 2:

The **pass-band** usually has less than 0.0003 dB of ripple from $0f_s$ to $0.2f_s$

Stop-band attenuation of greater than 90dB from $0.3f_s$ to Nyquist.

CIC



R = 7:

Frequency bands in the interval:

k/**M** f_c, k = 1, 2,… [R/2], f_c ~ $1/8f_s$

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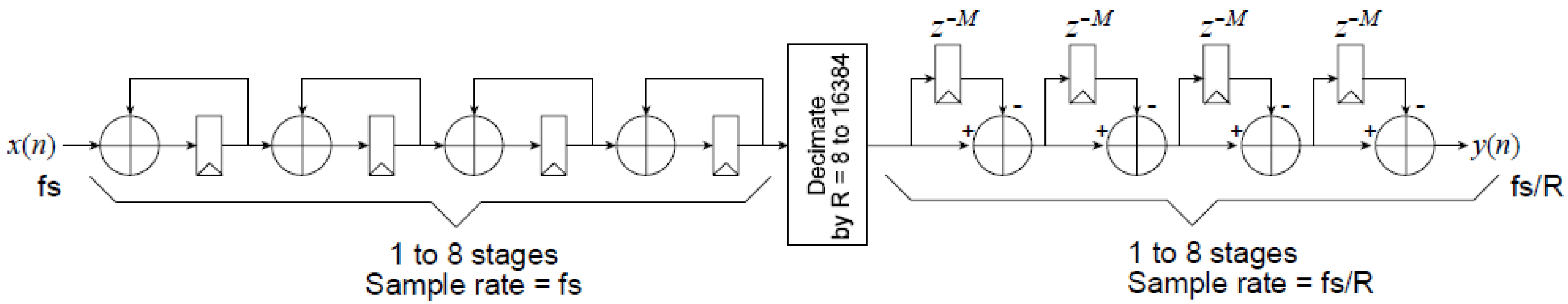
CIC-FILTERS

CIC – Cascaded integrator-comb

Basic characteristics of CIC-filters:

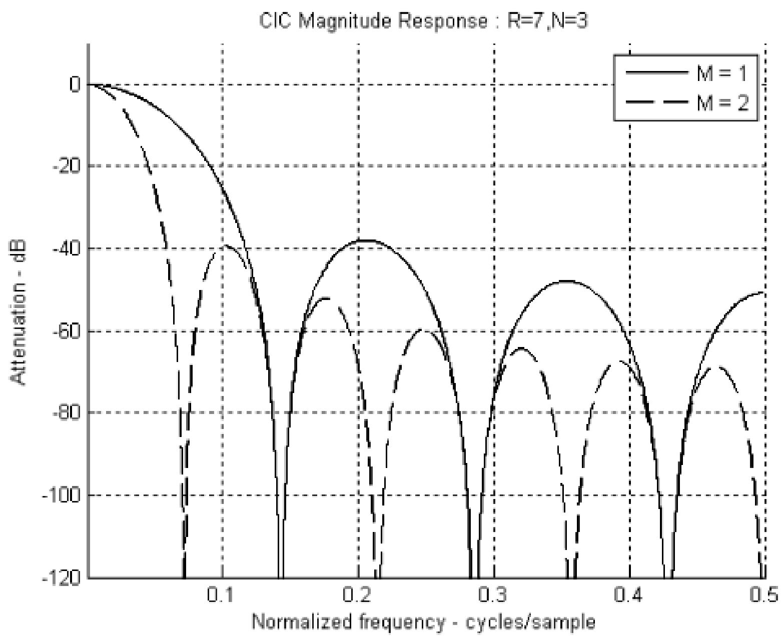
- **N** – number of CIC-stages
- **R** – decimation rate change
- **M** – differential delay in the comb section stages of the f



The implementation of this filter response with a clever combination of comb filter sections, integrator sections, and downsampling for decimation give rise to the hardware-efficient implementation of CIC-filters.

CIC MAGNITUDE RESPONSE

Effect of differential delay **M**:

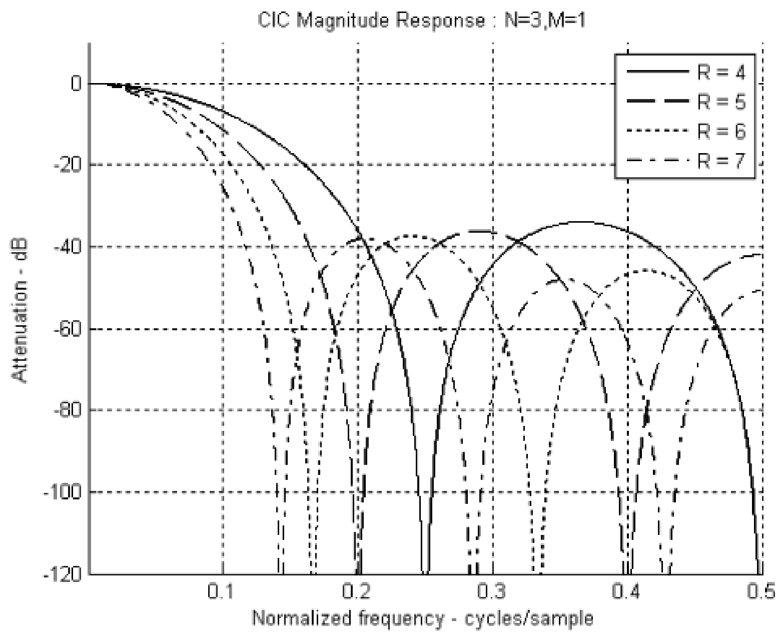


Normalized frequency is the discrete-time frequency, normalized to the higher frequency in a rate changing filter - input sampling frequency in a CIC decimation.

This shows the effect of the differential delay **M** on the magnitude response of a filter with 3 stages (**N** = 3) and a sample rate change **R** = 7. Besides the effect on the placement of the response nulls, increasing **M** also increases the amount of attenuation in side lobes of the magnitude response.

CIC MAGNITUDE RESPONSE

Effect of rate change **R**:

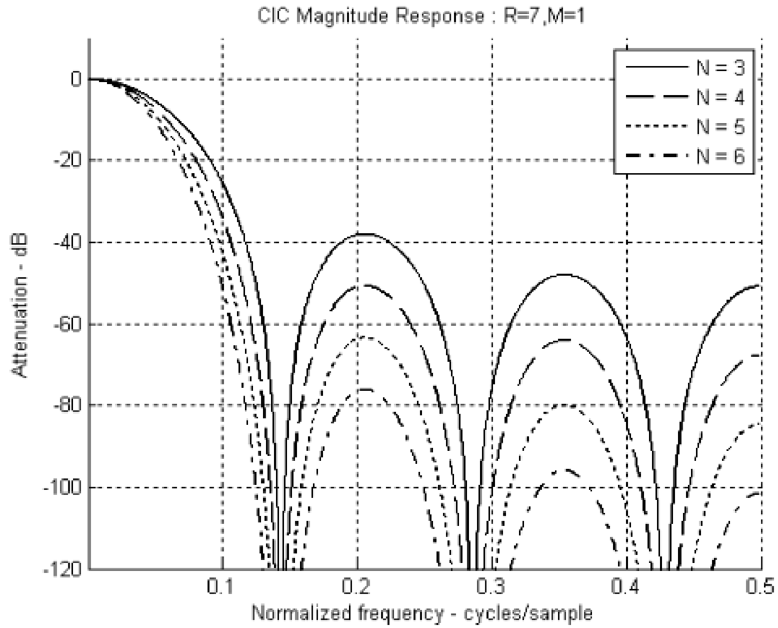


Normalized frequency is the discrete-time frequency, normalized to the higher frequency in a rate changing filter - input sampling frequency in a CIC decimation.

The effect of **R** on the magnitude response can be seen in this figure. In essence, increasing the rate change increases the length of the cascaded unit-amplitude, rectangular window of length **R*****M**. This results in an increase in attenuation and decrease of the width of the response side lobes.

CIC MAGNITUDE RESPONSE

Effect of number of stages N:



Normalized frequency is the discrete-time frequency, normalized to the higher frequency in a rate changing filter - input sampling frequency in a CIC decimation.

Increasing **N** has the effect of increasing the order of the zeros in the frequency response. This, in turn, increases the attenuation at frequencies in the locality of the zero. This effect is clearly illustrated in this figure where we see increasing attenuation of the filter sidelobes as **N** is increased.

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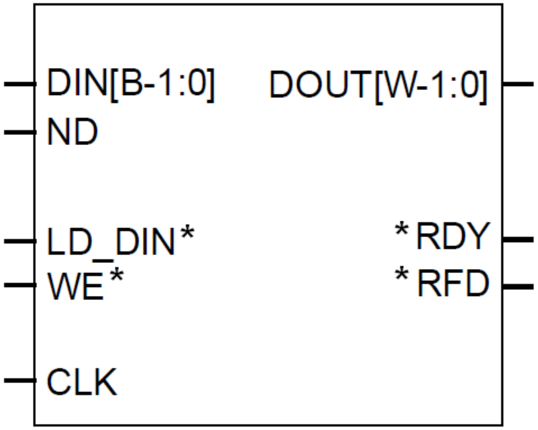
CIC CORE

Standard I/O interface of CIC core



*Optional pin

NAME	DIRECTION	DESCRIPTION
CLK	Input	Clock
DIN	Input	Data Input
ND	Input	New Data
DOUT	Output	Filter Output Sample
*RDY	Output	Filter Output Sample Ready
*RDF	Output	Ready for Data
*LD_DIN	Input	LD_DIN input bus
*WE	Input	Write Enable signal

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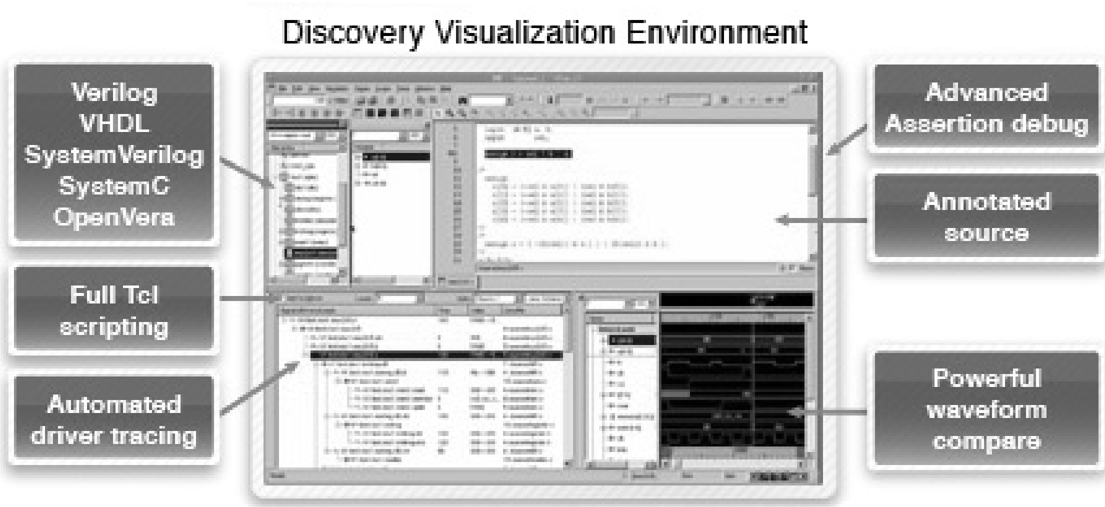
SIMULATION

Device and simulation parameters

HDL language: Verilog
EDA software: Design Compiler, VCS

Device parameters:

- **M** = 1
- **N** = 4
- **R** = 4
- **width input** = 8
- **width output** = 16



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SIMULATION

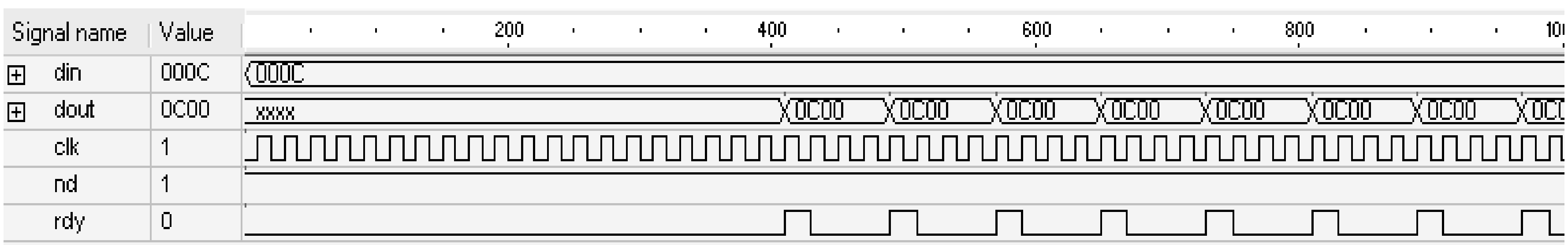
Checking main formulas

For CIC decimators, the gain **G** at the output of the final comb section is:

$$G = (RM)^N$$

If **Bin** is the number of input bits, then the number of output bits, **Bout**, is:

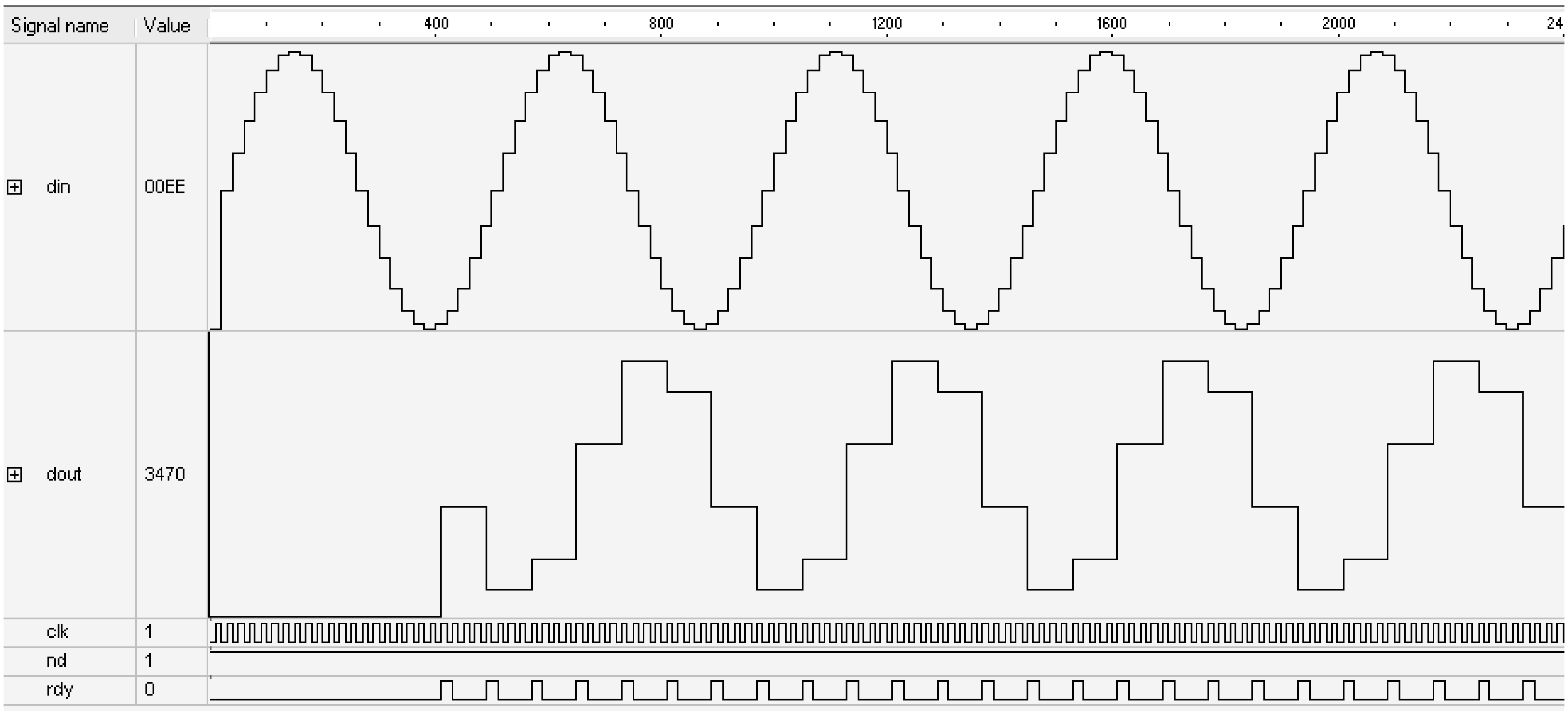
$$B_{\text{out}} = [N \log_2 RM + B_{\text{in}}]$$



$$C'h \bullet (4 \cdot 1)^4 = C00'h \quad (!)$$

SIMULATION

Simulation sinusoidal signal



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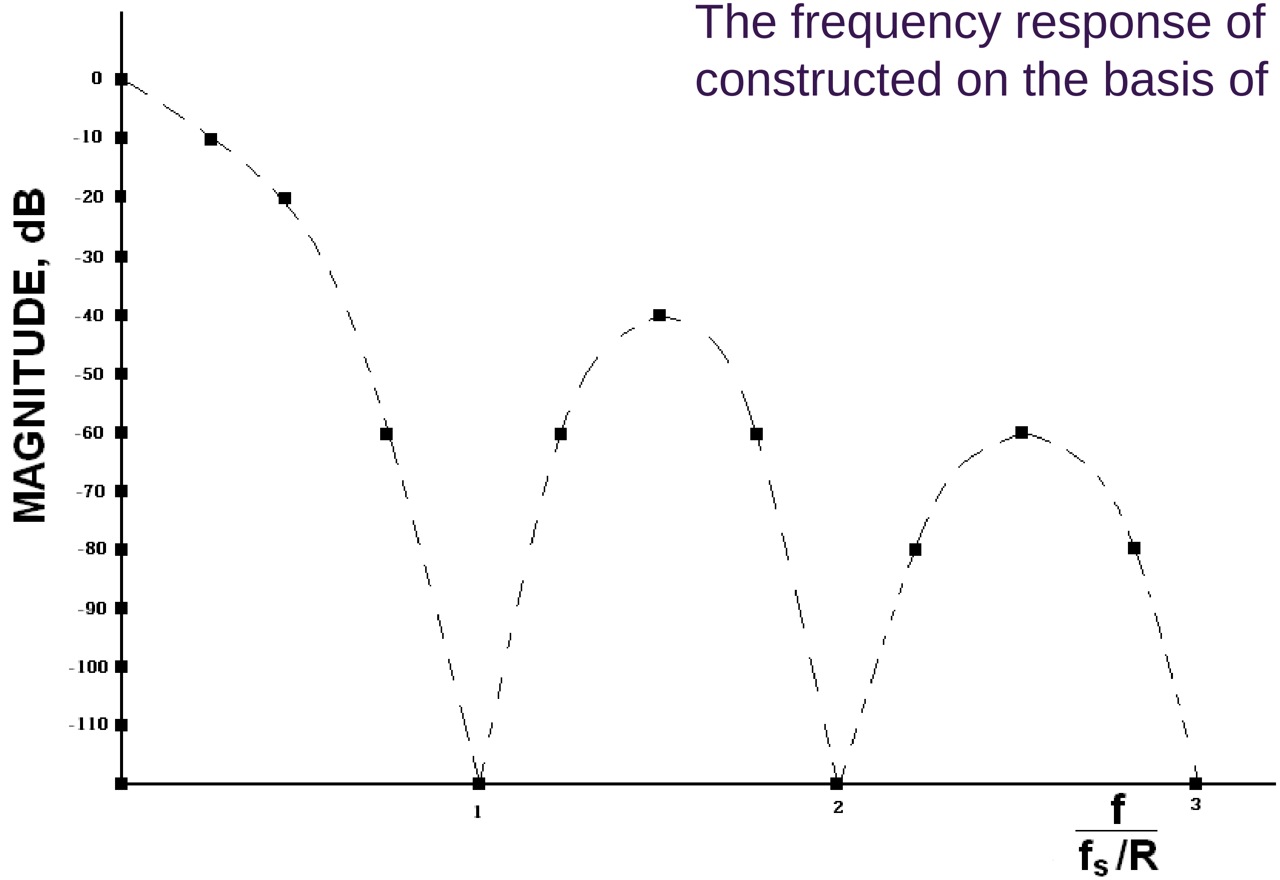
SIMULATION

Frequency response

The frequency response of designed device constructed on the basis of experiment



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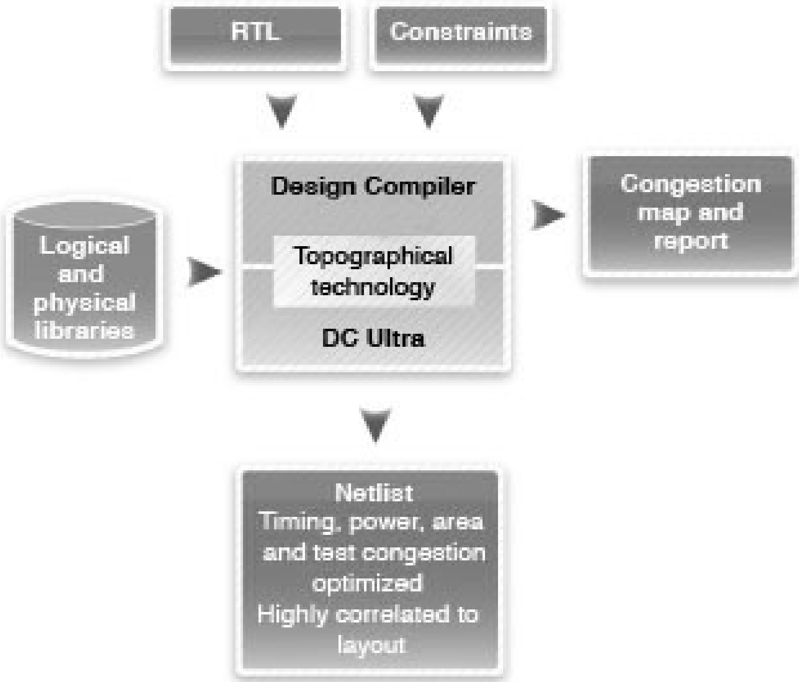
MAIN CHARACTERISTICS

All optimization is **off**.

Dynamic power consumption: **~830 μW / clock**

Area: **~12100 μm^2**

Max frequency: **~165 MHz**



APPLICATION

A CIC filter is typically used in applications where the system sample rate is much larger than the bandwidth occupied by the signal.

They are commonly used to build:

- DDCs
- DUCs

Some applications:

- radar systems
- cable modems
- satellite receivers
- 3G base stations

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THANK YOU

Thanks for your time and attention.

Are you questions?