

Характеризация высокоскоростных ячеек. Методы определения задержки. (High Speed Cells Characterization. Methods of the time delay measurement)

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Проведен обзор методов определения задержки применимых для характеристики быстродействующих ячеек.

INTRODUCTION

Problem of quality maintenance and reliability of very large scale integration circuit (VLSIC) is one of the most actual problem in modern microelectronics. The scientific basis of the decision of this problem are methods of technical diagnostics and testing, allowing to estimate conformity of technical parameters VLSIC to requirements standard – engineering specifications at design stages.

It is known that cells on which modern digital circuits are constructed are high speed operating cells. These cells require the accurate characterization. In high speed integrated circuits time delays on interconnects become critical. An approximate solution based on capacitive and RC models for simulation is often not appropriate to describe critical paths where delays under 100 ps are to be considered. In such cases, long interconnections should be considered as transmission lines placed over a highly dispersive material. With assisted by works of many scientists have developed models for accurate simulation of interconnect lines on semiconductor substrate. This paper presents methods of measure the delays between two interconnected points. The methods can be extended to on chip dynamic characterization of various complex cells operating at high speed.

In the timing analysis of a system composed of one or more transparent cells and the corresponding interconnection lines, when high speed digital signals are passing through that path, the rising and falling transition times (t_r , t_f) and the propagation time (t_p) -(Fig.2)- are significant parameters. The delay of the signal between the net 2 and 3 or net 1 and 3 was analyzed (Fig.1), assuming that X1 and X2 are simple inverters.

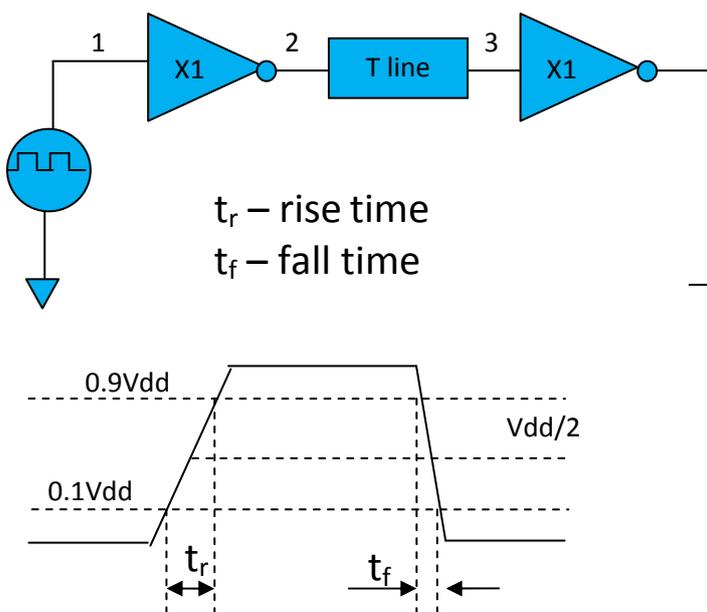
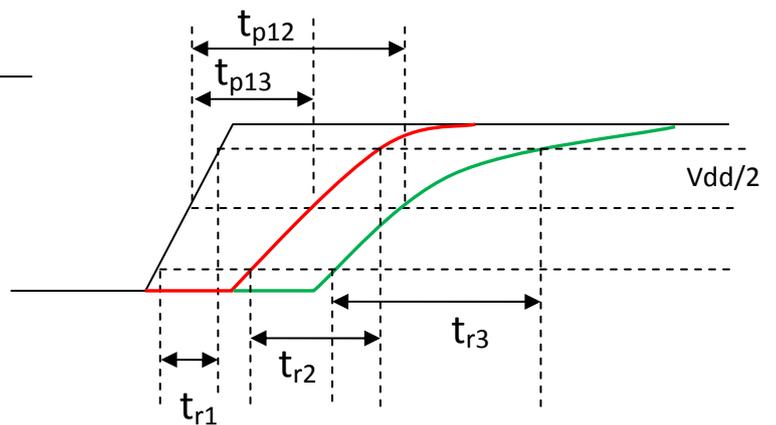


Figure 1



$t_{r1/r2/r3}$ – rise transition time at net 1/2/3

t_{p12} – propagation time between net1 and net 2

t_{p13} – propagation time between net1 and net 3
(path delay)

Figure 2

Combined with an analysis of a digital signal according to its switching transition time, a frequency spectrum of interest can be determined.

Moreover, in developed models, the delay between net 2 and 3 is not only dependent on the line characteristics, but it is also a function of the signal injected (at net 2-Fig.1). The transition time of that signal is itself a function of the input signal at net 1 and of the transfer function of the cell X1. In a real case, the load at X1 output is a complex impedance, which is a function of X2 input impedance reflected through the transmission line.

To summarize, at high frequencies, it is difficult to separate the delay introduced by X1 from the transmission line characteristics, because of the sensitivity and the non-linearity of the system with respect to input signal characteristics. The delay introduced by the two elements (active cell X1 and interconnection) are mutually dependent. A possibility to analyze the system composed of X1 and a long interconnect line is to measure the delay time between net 1 and 3 (Fig.1) that we call “path delay”. It is a natural way to represent “path delay”, because it corresponds to the time necessary for a signal to act in a following logic stage. The “path delay” combines the propagation and the transition time of the signal, taking into account parasitic elements.

The rest of the report proposes three methods for measuring the path delay.

THE RING OSCILLATOR PATH DELAY MEASUREMENT METHOD

The first method is the ring oscillator path delay measurement method. The basic idea is to introduce a replica of the path segment we wish to measure in a ring oscillator. This increases the oscillation period, which allows measure any complex transparent path in its realistic environment. The proposed module contains a symmetrical ring oscillator as shown in fig.3.

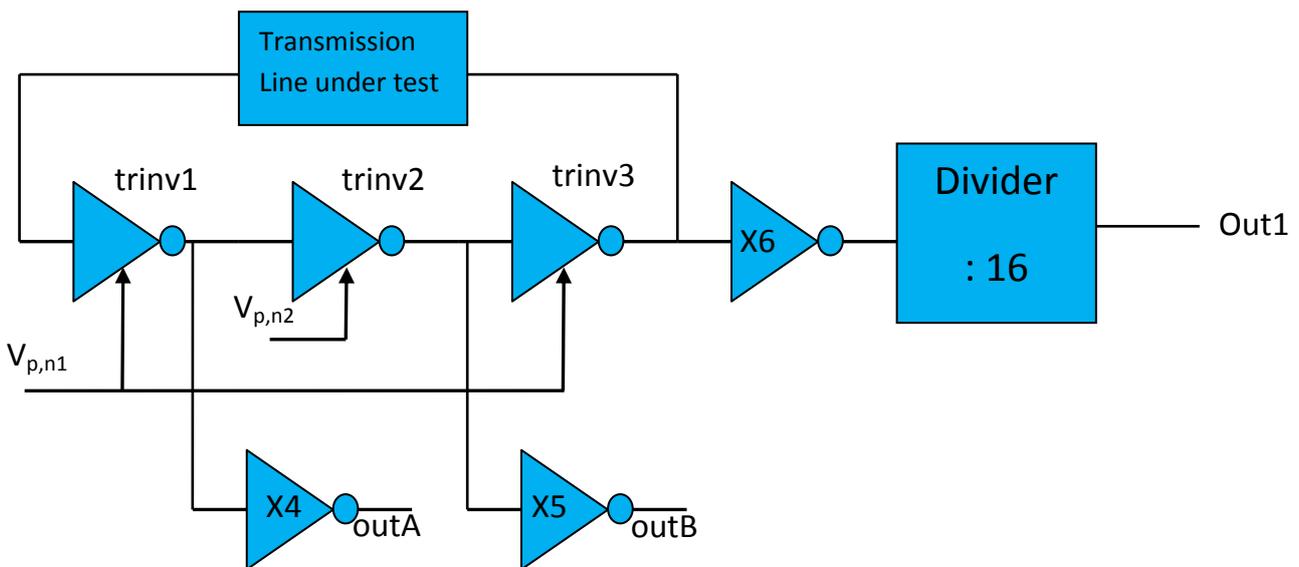


Figure 3 – Ring oscillator based path delay measurement structure

The “trinv” cells are CMOS inverters which allow to vary the free oscillation frequency via two DC control voltages V_p , V_n . Two separate frequency control lines ($V_{p,n2}$) are used for the second inverter in the chain. This allows change the free running period while the two terminations on the transmission line are held constant. A similar oscillator is used for calibration, and in this case we use very short connections between inverters. Other similar oscillators use different configurations for the line connecting stage 3 and stage 1. The circuit also contains a divider by 16 implemented with dynamic TSPC latches.

Once divided by 16, the signal can be propagated through chip I/O pins to conventional test equipment. The inverters X4,X5 are necessary to balance the load on each “trinv” cell, and to spread the generated signal to other blocks like the phase detector “phdet” described in the next section. The signal period measured for the reference oscillator is

$$T_1 = 2(t_{pr} + t_{pf})_{trinv1} + (t_{pr} + t_{pf})_{trinv2}, \quad \{1\}$$

where the period is expressed as a function of propagation delays experienced by the rising and falling transitions. Under specified $V_{p,n1}$ and $V_{p,n2}$ DC control levels and for $V_{p,n1}=V_{p,n2}$

$$(t_{pr}+t_{pf})_{trinv1} = (t_{pr}+t_{pf})_{trinv2} \cdot \quad \{2\}$$

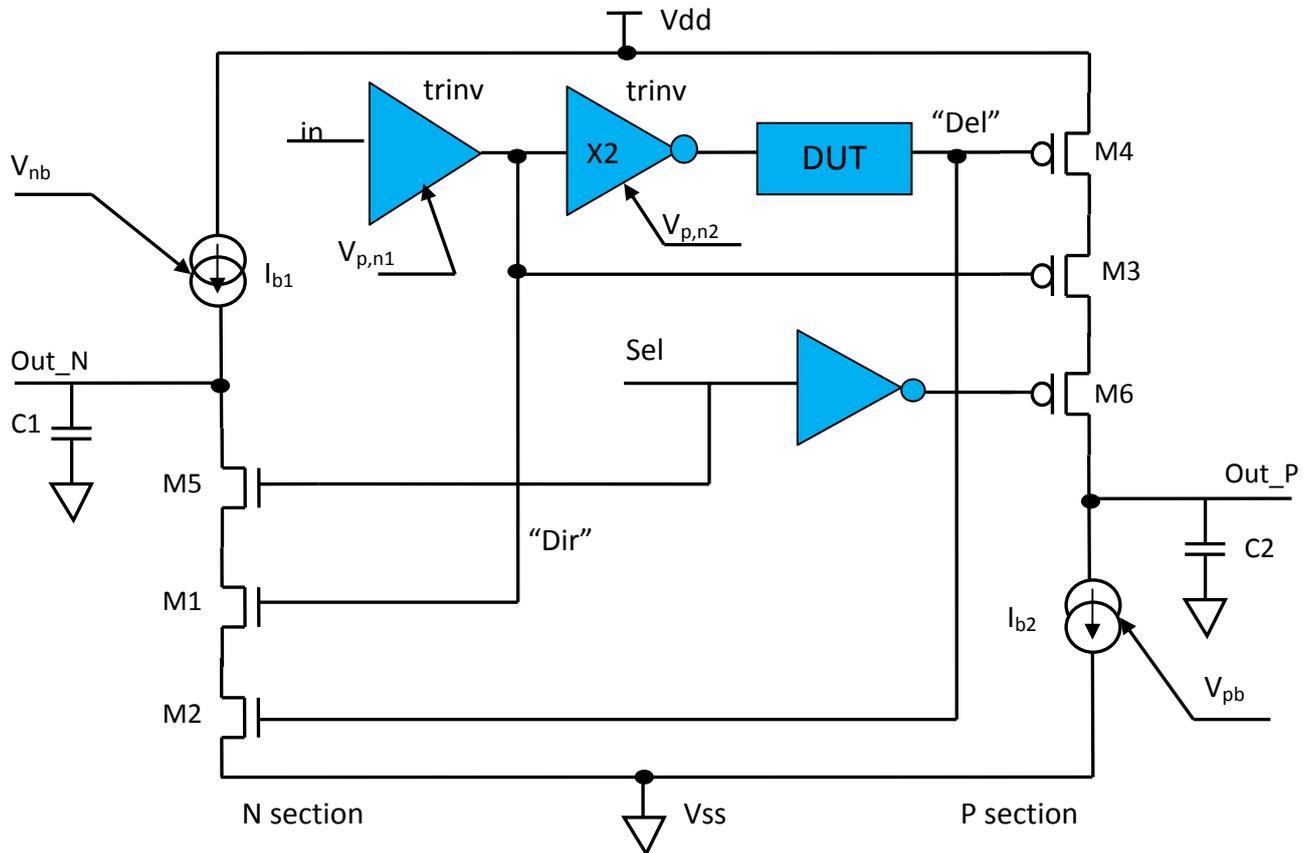
In general we may define

$$T_0=(t_{pr}+t_{pf})_{trinv1} + (t_{pr}+t_{pf})_{trinv2} \cdot \quad \{3\}$$

By using these modules we can measure the sum of the rise and fall propagation times, but we cannot differentiate them. In order to obtain these parameters separately, we propose the signal phase detection module as described in the next section.

PHASE DETECTION MODULE

The second method is measure delay by phase detection module. At low frequency, the conventional XOR is a valid digital module for phase detection. When the speed of the signal increases and the propagation time gets comparable to the period of the signal, the XOR gate becomes in operant for that purpose. However, the concept of phase detection remains valid and with the phase detector shown in Fig.4., we can measure small phase differences between a direct signal (Fig.4-net “Dir”) and its reversed and delayed version (Fig.4-net “Del”). This phase detector is fed by an input signal “in” coming from an oscillator such as those presented in previous section (Fig.3 - outA or outB).



DUT – device under test (transmission line or cell)

Figure 4 – The phase detection module “phdet”

The module contains two sections N and P, where the input signal, amplified by X1(Fig.4), is injected in the gates of the M1 and M3 transistors, passed through X2 and the DUT (any non-inverting transparent circuit), and then fed to the gates of transistors M2 and M4. If the capacitors C_1 , C_2 used here as integrators are not connected, the output signal of the “phdet” cell- out_P , out_N - are determined by the phase difference between the signals. The information on the rising transition is extracted from the P section on out_P , whereas out_N, and the N section reflects the characteristics of the falling transition.

Since the fine characteristics of the signal on out_N and out_P would not propagate through a regular IC pad, we average them with C1 and C2. The information is thus extracted as the variation of the DC values of out_N, and out_P.

The current sources I_{b1} , I_{b2} are controlled by V_{nb} , V_{pb} bias DC voltages (separate from $V_{p,n1}$, $V_{p,n2}$). The output of several such “phdet” modules are connected in parallel, and they are activated by a suitable selection mechanisms. As in the ring oscillator method, we use two “phdet” blocks for calibration purposes. The DUT in these blocks are the lines with different lengths when we try characterize the effects of long interconnects for instance.

The principle of operation consists in measuring the period of the two oscillators in certain control voltage conditions to extract the overall path delay lines. Then, using two “phdet” modules, we measure the DC output voltages whose values separately reflect the propagation of the path delay apart in the rising and falling transitions.

BUILT-IN SELF-TEST METHOD

The third method is built-in self-test method. A built-in self-test (BIST) method and apparatus for digital integrated circuits (ICs) and for systems, including multiple ICs, measures signal propagation delays in combinational and sequential logic, set-up and hold times, from any circuit node to any other circuit node including pin-to-pin and from one IC to another. The IC under test is provided with two test bus conductors passing near every circuit node of interest and connected there to by switches or buffers. During test, an oscillator is created including the test bus, a constant delay, counters, and a delay path of interest or a reference path. The delay path of interest may include e.g. an analog filter. The oscillation period of the oscillator when the reference path is selected is subtracted from the oscillation period when the oscillator includes a delay path of interest. A delay copier copies the delay between any two signal events, without injecting any test signal into the circuit under test (e.g. on-line test), and the delay copy can be measured by selecting it in the oscillator. The example only one delay path presented on slide 6.

This method also directed to built-in measurement of delays in ICs using only a single externally provided constant frequency as an absolute time reference. This facilitates verification of on-chip delays for new designs, sorting of fast and slow digital ICs for premium pricing, and testing for delay faults caused by defects in unlocked combinational logic, asynchronously clocked logic, gated-clock logic (e.g. ripple counters), paths from an input pad to an output pad, and paths which affect set-up and hold times.

CONCLUSION

In conclusion I want to say that all of these methods are successfully applied in practice for characterization cells on the test chip (in silicon). Each method has some advantages and disadvantages. The ring oscillator path delay measurement method is the simplest and cheapest of the presented methods. Therefore, many companies using it for the characterization and testing of the standard cells libraries in silicon. It is known that many of current digital library contain a large number of elements today, for example N-cells (in practice it is about two or three hundred cells). To test this library, you will need to build N ring oscillators, for each of the library elements. It means that you should pass on a standard process design floor (which presented on slide 7) of 200-300 times. This takes a lot of time. Therefore the design of ring oscillators is topical issue. Currently I solve this problem within the framework of my dissertation. Automation is carried out through the Perl and TCL languages.

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