

Modeling of total dose radiation effect of RF PD SOI-MOSFET using Sentaurus TCAD

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Modern integrated circuits (VLSI) utilize SOI-structures and SOI-MOSFETs.

Such SOI - transistors have many advantages in comparison with bulk devices:

- lower drain and source capacitances and high performance for digital and RF-applications
- full dielectric insulation of each transistor, low leakage currents, even at high operating temperatures, no latch-up in CMOS structures
- smaller layout dimensions
- higher immunity to total dose radiation and single event upsets (SEU)

This paper presents characterization of partially-depleted A-type SOI – N-MOSFET with different channel dimensions using Sentaurus TCAD

It is necessary to:

- perform two-dimensional simulation of basic process flow and create three-dimensional A-type SOI - device structure with different channel length $L=0.35$ and 0.5 μm and width $W=1,2,3$ μm
- perform DC-device simulation: simulate static current-voltage characteristics ($I_d(U_{gs})$, $I_d(U_{ds})$)
- perform AC-device simulation: simulate small-signal dependences of Current Gain (H_{21}) and Mason's Unilateral Gain versus frequency
- calculate dependences of Unity Gain Frequency (f_1) and Maximum Frequency (f_{max}) versus gate-to-source (U_{gs}) and drain-to-source (U_{ds}) voltages
- calculate dependences of device off-state leakage current (I_d) versus radiation dose (Dose) using device simulation

Simulation of basic DC characteristics has shown that the front gate threshold voltage is about 1V, and the back gate threshold voltage is about 90V. Simulated output current-voltage characteristics ($I_d(U_{ds})$) of transistors with different channel length and source width define the operating point for small-signal frequency analysis: $U_{ds}=2\text{V}$, $U_{gs}=1-4\text{V}$.

Simulation of AC characteristics has shown that at the bottom of the slide we can see following:

- $f_1 = 24$ GHz for $L=0.35$ μm and 17 GHz for $L=0.5$ μm
- $f_{\text{max}} = 57$ GHz for $L=0.35$ μm , and 43 GHz for $L=0.5$ μm

So such devices can work as amplifiers at frequencies higher than 2 GHz.

Next let's consider total dose effects.

It is well known, that during radiation, positive charge trapping occurs in oxides of SOI-structure, changing the potential distribution and lowering the back gate threshold voltage

In order to simulate oxide charge trapping under radiation, it is necessary to define oxide as semiconductor with oxide properties. Also user must define maximum concentration of neutral traps in oxide (C_{trap}). This value strongly depends on oxide fabrication conditions. For BESOI structures this value $C_{\text{trap}} \leq 3 \cdot 10^{17} \text{ cm}^{-3}$.

Simulation of total dose accumulation effect leakage currents of SOI-MOFSETs was carried out for 3D – structure with fixed body (the best case) and for 2D – structure with floating body (the worst case). In all transient simulations, positive drain-to source voltage rises from 0 to 2 V at first second (s). Then the irradiation was considered during 20 s. The dose rate was 100 krads/s. The maximum trap concentration in oxide (C_{trap}) was a parameter ($10^{17} - 10^{20} \text{ cm}^{-3}$).

It was shown the drain leakage current rises only if C_{trap} is higher than 10^{18} cm^{-3} . This value is higher than C_{trap} for BESOI – structures. So we can consider that all our transistors, even without body contact – are radiation hard