Design Tools for Reliability Analysis

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Overview

- Introduction and Background
- Phenomena affecting Reliability
- Modeling Reliability phenomena
- Simulating Reliability effects
- Examples of some Reliability Simulators
- Conclusion

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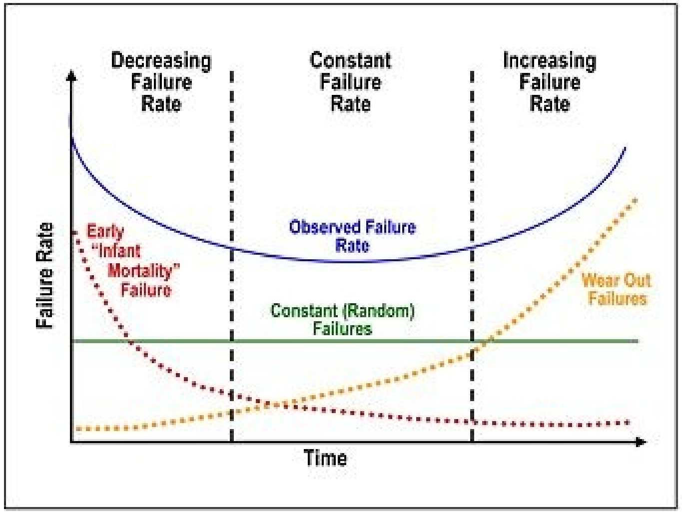
Understanding Reliability

- What is reliability?
  - Ability of a system to maintain its functionality even in unexpected circumstances
  - … to maintain functionality under stated conditions for a specified period of time (IEEE def.)
- Mostly concerned with aging effects in the context of semiconductors

Understanding Reliability (2)

- Typical Reliability Profile
- Infant Mortality
  - Burn-in Testing
  - Accelerated stress and elevated operating conditions



- Normal Operating Life
  - Stringent verification, immunity to soft errors
  - Safety margins
- Wear out
  - Design for Reliability paradigm
  - Safety margins

Motivation and Need for Reliability Analysis

- Why bother about reliability analysis?
- Profitability, Reputation, etc
- Shrinking design margins
- To avoid overestimation and being too pessimistic
- Pressure to deliver ever more performance
- Increasing contribution of secondary effects
- Increasing integration density and complexity

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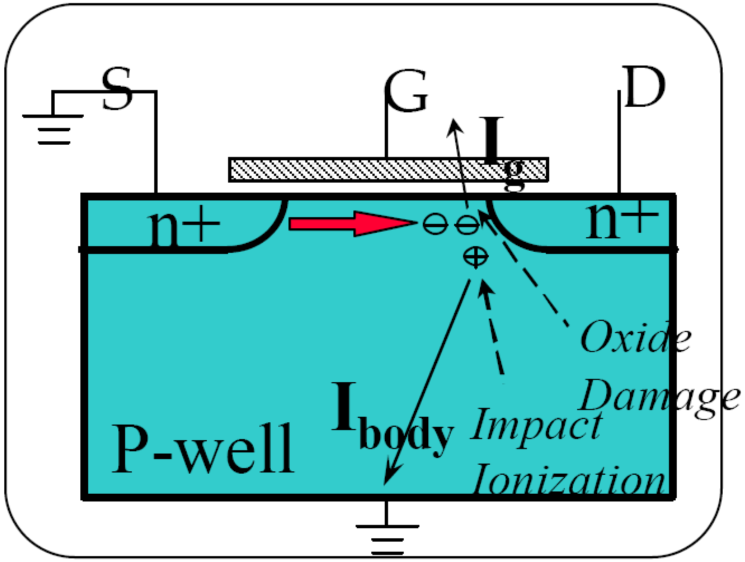
Physical Phenomena Affecting Reliability

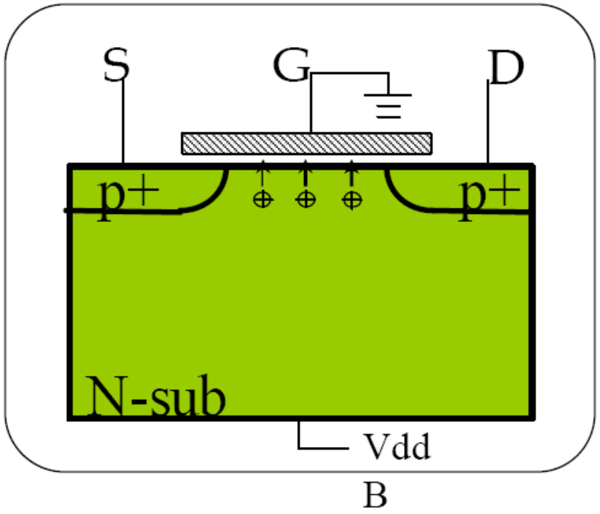
- Transistor Degradation
  - Hot Carrier Injection (HCI)
  - Negative Bias Temperature Instability (NBTI)
- Transistor Failure
  - Field Oxide Breakdown
- Interconnect Degradation
  - Electromigration (EM)

Hot Carrier Injection (HCI)

- High lateral electric field
- Injection into oxide
  - Interface state generation
  - V_{th} increases, I_D decreases
  - Transistor becomes slower
- Impact ionization
  - I_D increases, I_{body} increases
- Occurs in both NMOS and PMOS
- Severe for short channel and high I_D transistors at high V_D and low temperatures

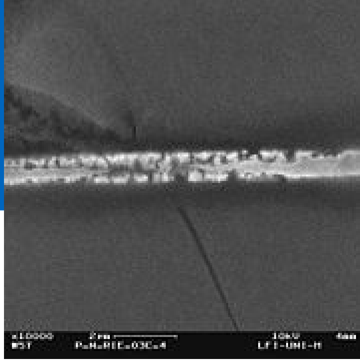


Negative Bias Temperature Instability (NBTI)



- Occurs only in PMOS
- High vertical electric field
- Complex electro-chemical phenomenon
- Trapping of holes into oxide
- Interface state generation
- V_{th} increases, I_D decreases, transistor becomes slower
- Severe for thin oxide transistors and at high temperatures

Electromigration (EM)



- High current density
- Metal atoms permanently displace and form voids
- Severe for
  - Al than Cu wires
  - DC than AC currents
- Poses limits to safe current densities (DC, AC, peak)
- Black's equation

$$MTTF = \frac{A}{J^n} e^{\frac{E_a}{kT}}$$

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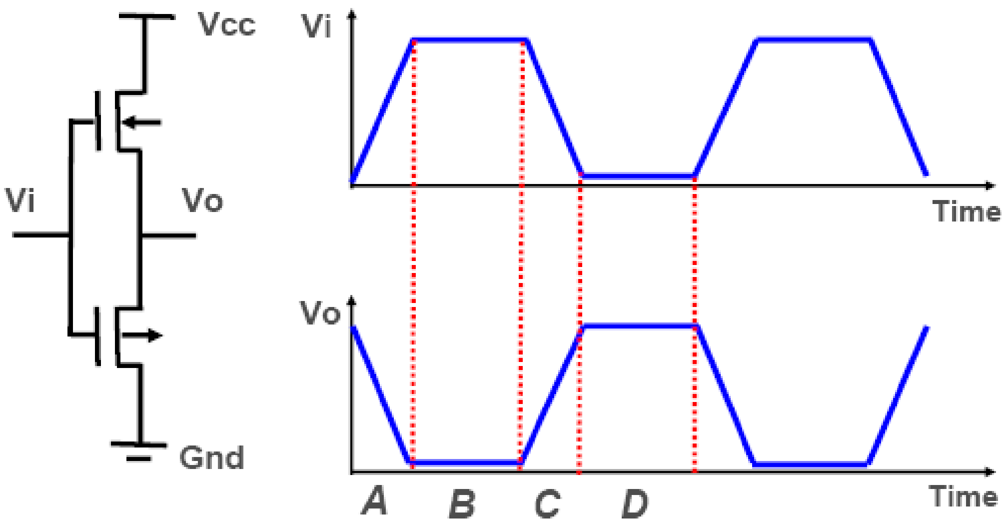
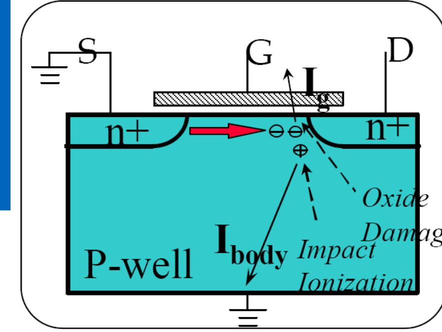
HCI and NBTI

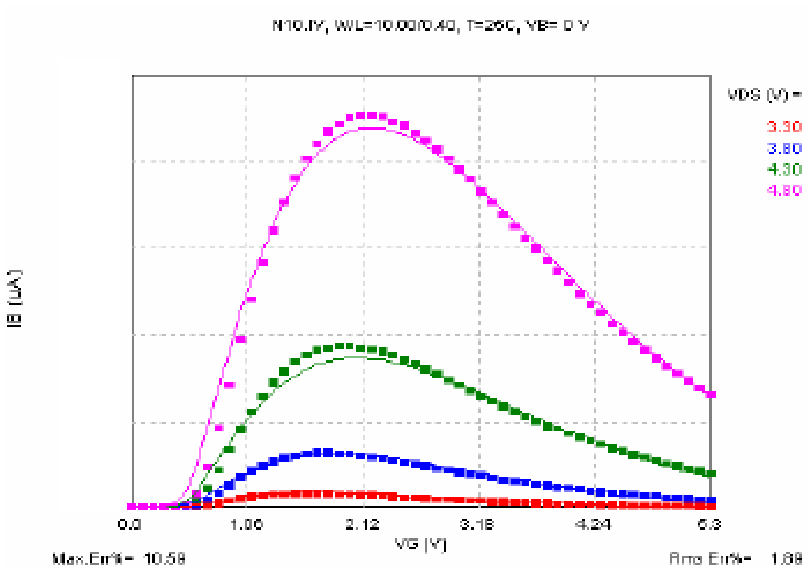
- HCI is active when I_D flows
- NBTI is active when PMOS is on
- Degradation is accumulative and pattern dependent
- Must be de-embedded from each other for modeling
- Typical effects are
  - V_{th} degradation
  - I_D degradation

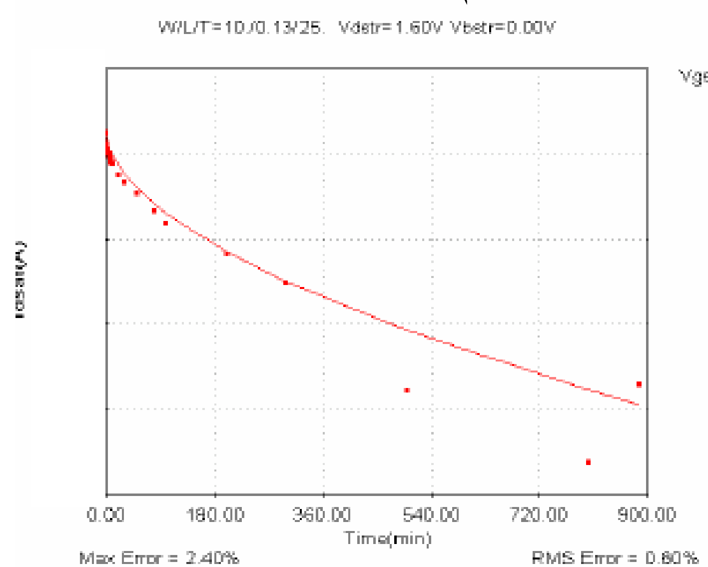


HCI Modeling

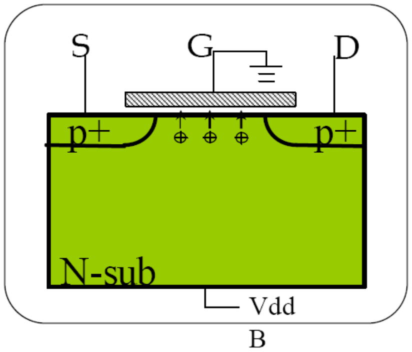


- I_D and I_{body} are good monitors
- A unified parameter is defined as, $AGE(\tau)=\int_0^{\tau}\frac{I_{body}}{H\cdot W}\left(\frac{I_{body}}{I_D}\right)^m dt$
- Degradation in I_D is modeled as, $I_{Dsat}(\tau)=I_{Dsat}(0)\left[1-(AGE)^n\right]$
- Accurate modeling of, $I_{body}=\frac{A_i}{B_i}(V_{DS}-V_{DSsat})\cdot I_D\cdot\exp\left(-\frac{B_i\cdot L}{V_{DS}-V_{DSsat}}\right)$





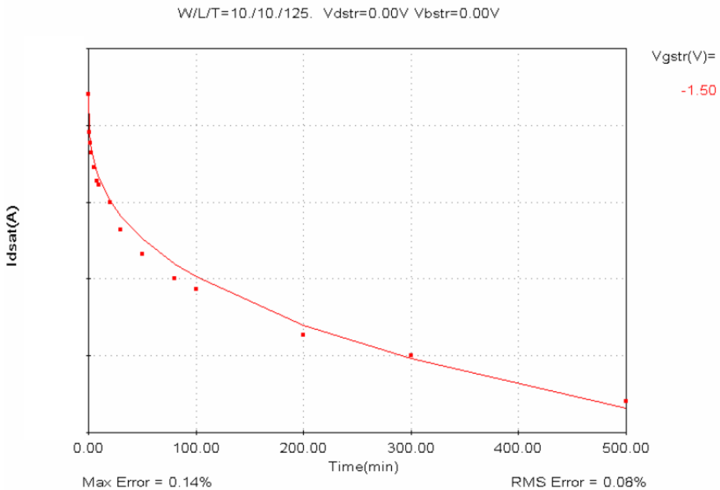
NBTI Modeling



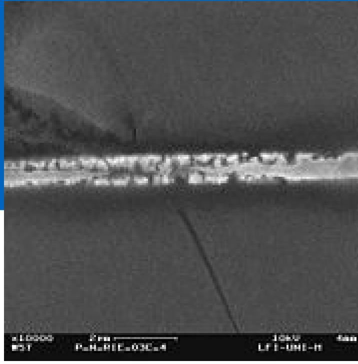
- NBTI AGE is defined as,

$$AGE(\tau) = \int_0^{\tau} \sqrt[n]{A \cdot \exp\left(-\frac{\Delta H}{k \cdot T}\right) \cdot \exp\left(-\gamma V_{GS}\right)}\, dt$$

- Degradation in I_D is modeled as, $I_{Dsat}(\tau) = I_{Dsat}(0)\left[1 - (AGE)^n\right]$
- NBTI Degradation is recoverable under AC stress
- Must avoid overestimation



EM Modeling



- Determination of worst-case current densities (DC, AC, peak)

- Static Methods (for digital circuits only)
  - Using switching pattern probabilities
  - Current drawn by logic gate, $I = \frac{C_L \cdot V_{DD}}{t}$

- Dynamic Methods (more accurate)
  - Application of stimuli to trigger worst-case currents

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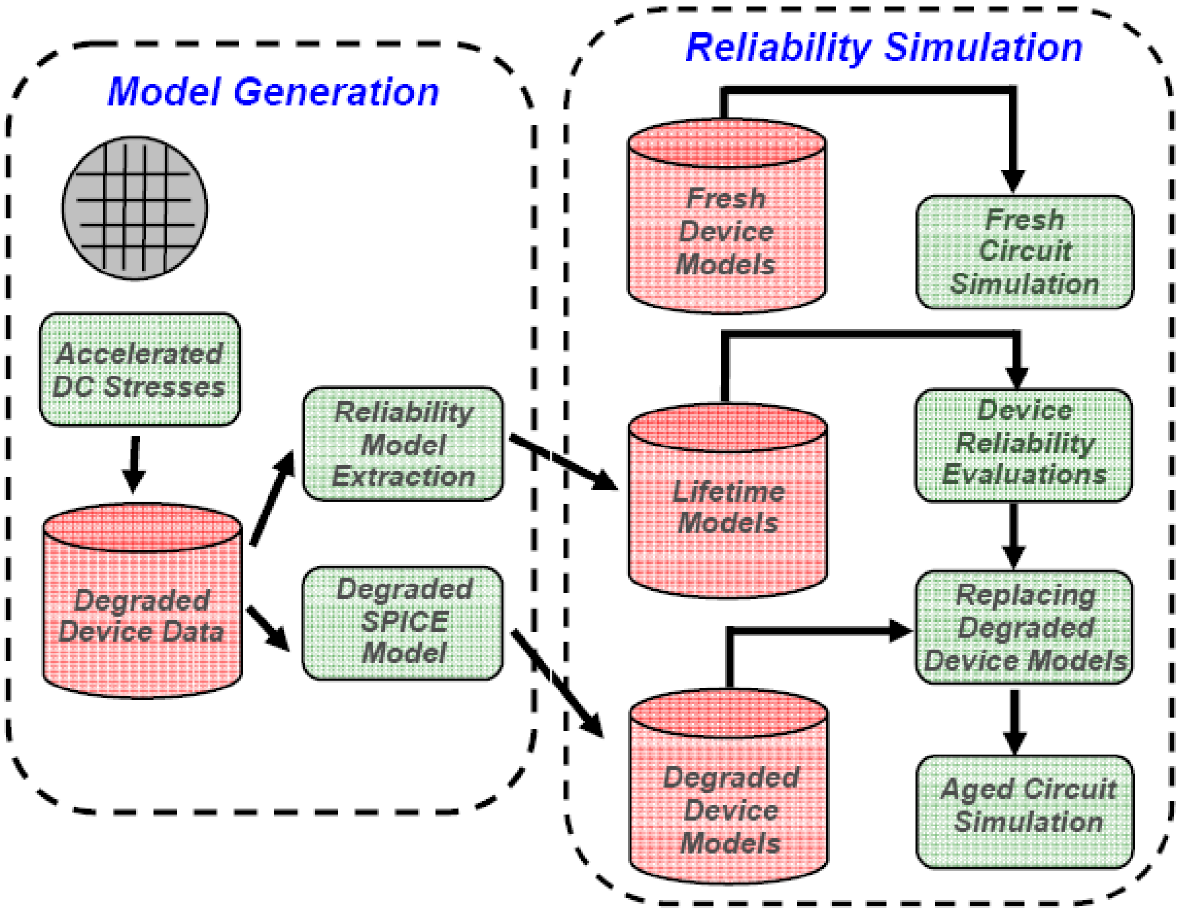
Basic Reliability Simulation Setup



Simulation Possibilities

- Simulation of aged device or circuit
- Exploration of degradation–tolerant circuits
- Device level reliability simulation
- Gate level reliability simulation
- Hierarchical simulation

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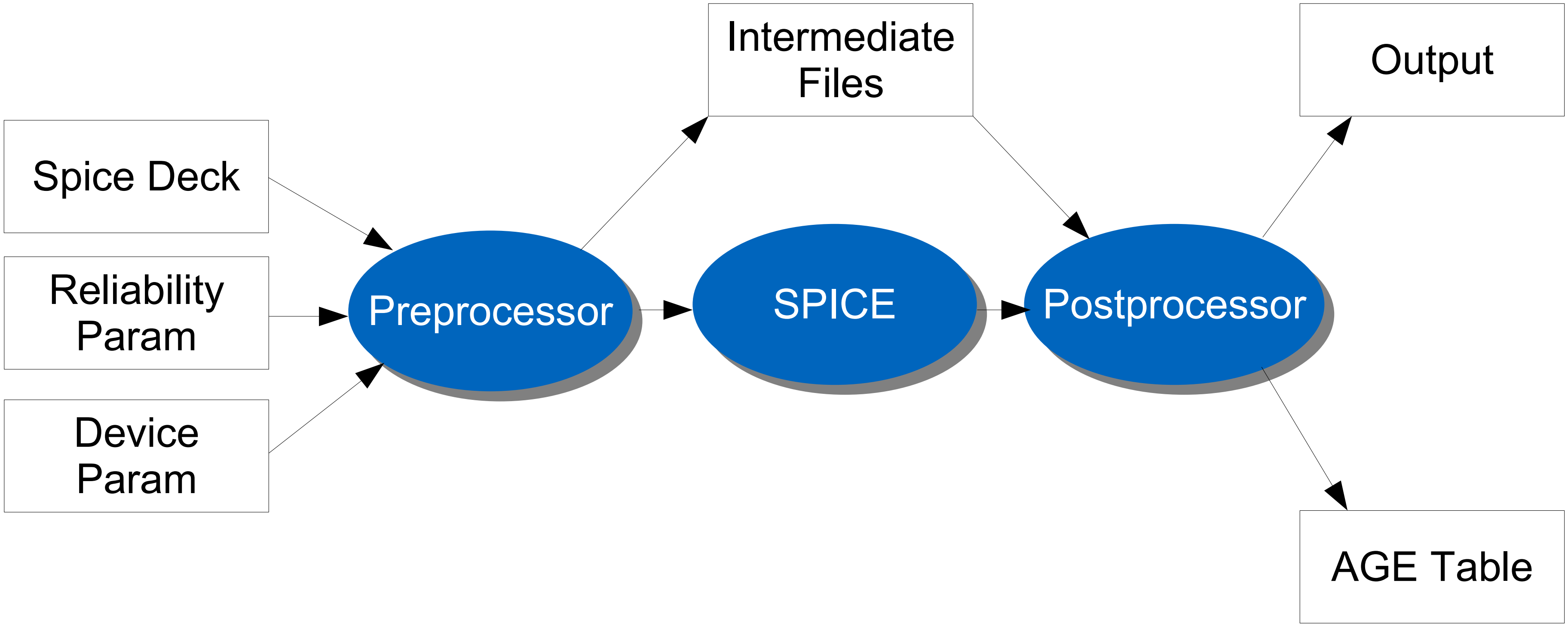
BERT – Berkeley Reliability Tool

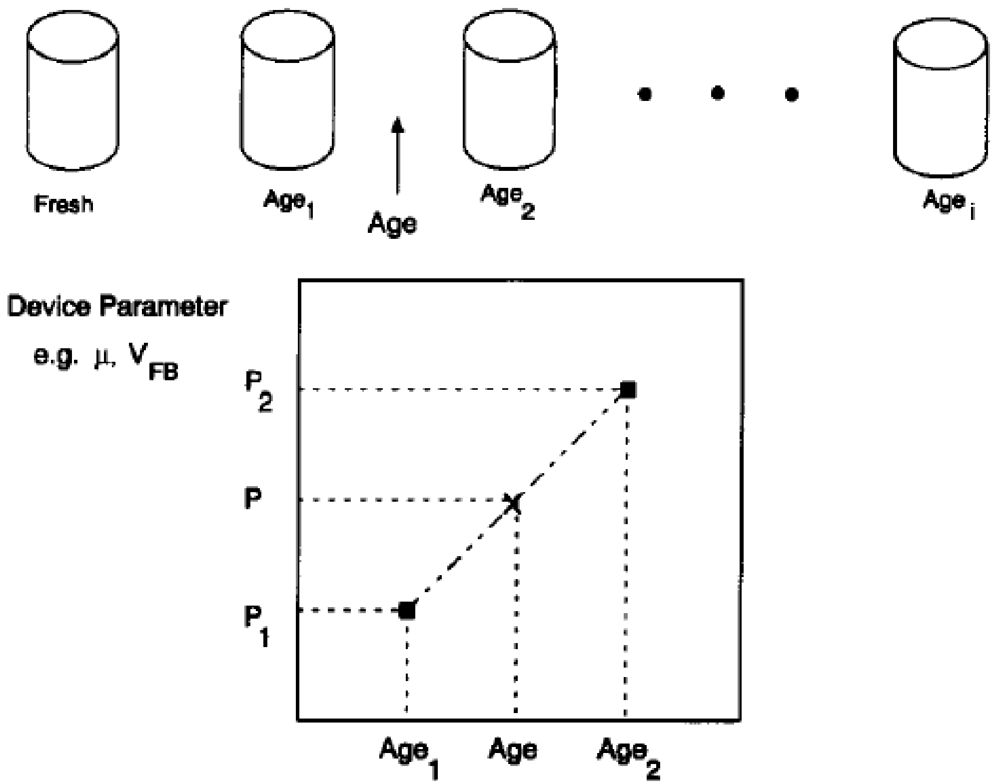
- Modular Design
- Circuit Aging Simulator (CAS)
- Circuit Oxide Reliability Simulator (CORS)
- EM (Electromigration)
- BiCAS (Bipolar Circuit Aging Simulator)

BERT Simulation Flow



BERT Simulation Flow (2)

- Aged device models come from burn-in testing
- Interpolation is used to generate required aged device models

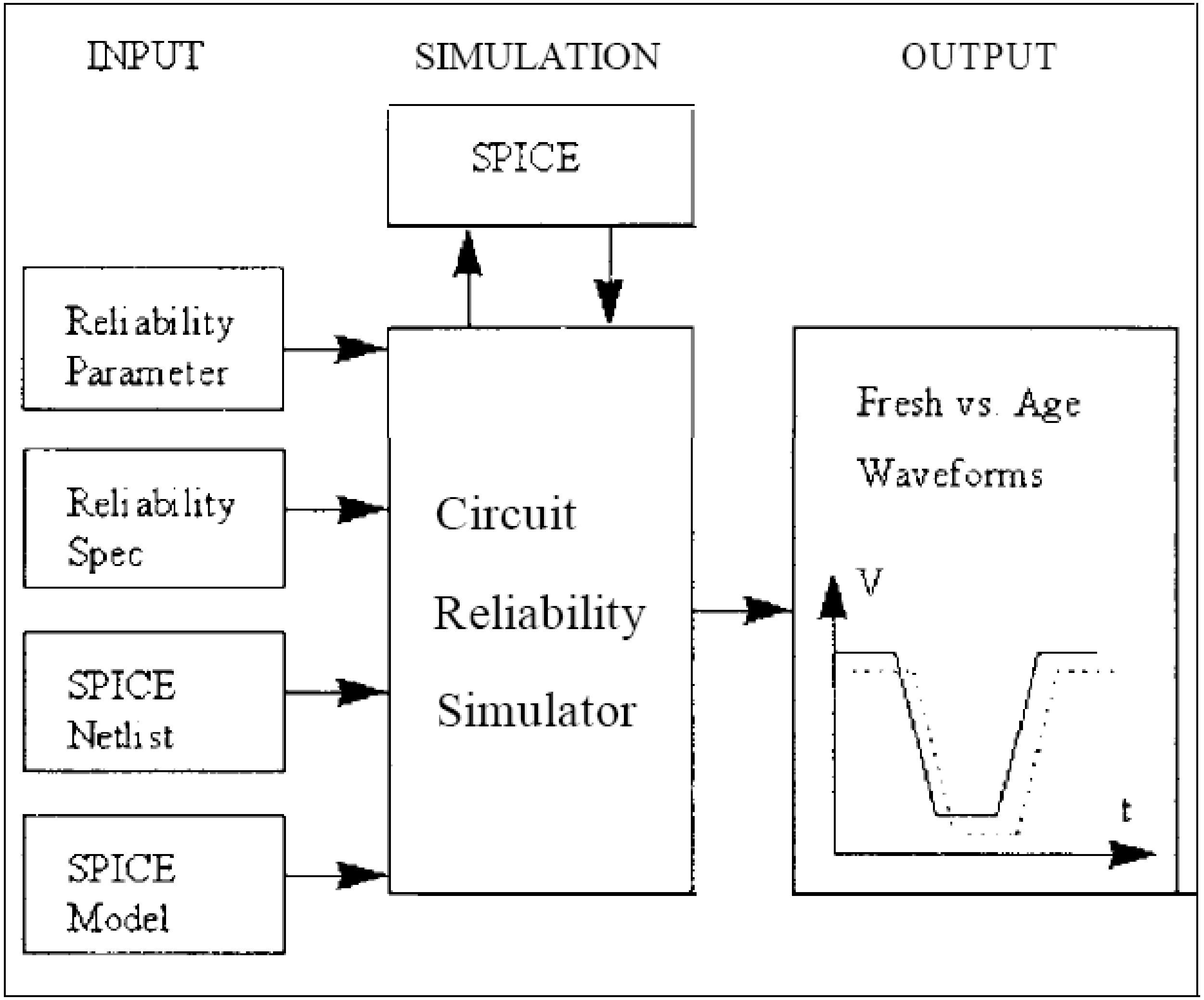


GLACIER

- Gate Level Circuit Characterization and Simulation System for Hot Carrier Effects
- Based on gate level delays of aged circuits

$$\alpha(T_{slew}, C_L, N_{sw}) = \frac{T_{aged}}{T_{fresh}}$$

GLACIER Simulation Flow



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- Increasing importance of reliability analysis
- Better understanding and modeling of reliability phenomena
- Burn-in testing and aged device model extraction
- Development of Tools
- Design for Reliability Paradigm

Thank you